LED growth compatibility between 2”, 4” and 6” sapphire

Sapphire substrate diameters of 2”, 4” and 6” with different thicknesses have been investigated by Veeco Instruments Inc for GaN-based blue LED (460nm) MOCVD epitaxy. Growth processes equivalent to standard 2” growths have been achieved for 4” wafers with thicknesses of 650 and 900μm as well as 6” wafers with a thickness of 900–1300μm. However, the quality of the 6” processes has shown a strong dependence on wafer thickness. By understanding the factors affecting the thickness and wafer bow dependence during epitaxial growth, process conditions can be modified to provide equivalent performance on 4” and 6” wafers.

The LED industry is aggressively reducing manufacturing costs to compete economically with existing lighting technologies. One approach currently being pursued is to produce LED epitaxial growth on larger-diameter wafers such as 4″ and 6″ sapphire substrates. Epitaxy on 4″ substrates is in pilot production, and 6″ wafer sizes are being explored, as they are compatible with existing silicon fabrication line equipment. Unlike the 2″ to 4″ transition, epitaxial growth on 6″ has proven to be more challenging, primarily due to the large thermal and lattice mismatches that occur between the sapphire and gallium nitride (GaN) layers, which result in large bowing of the wafers throughout the process.

We have developed a simple standard LED process in our 465mm chamber, and have used it to compare differences in 2″, 4″ and 6″ wafer configurations. The 2″ and 4″ processes exhibit good compatibility, but 6″ processes require additional work to adjust wafer curvatures, especially when working with thinner substrates. In this paper, we briefly cover the compatibility of 2″ and 4″ processes, and then focus on the more recent 6″ process development. In all cases, the growth environment (laminar flow conditions, temperature and pressure ramps) remain constant across all wafer sizes; the primary difference between experiments is the wafer carrier pocket geometry.

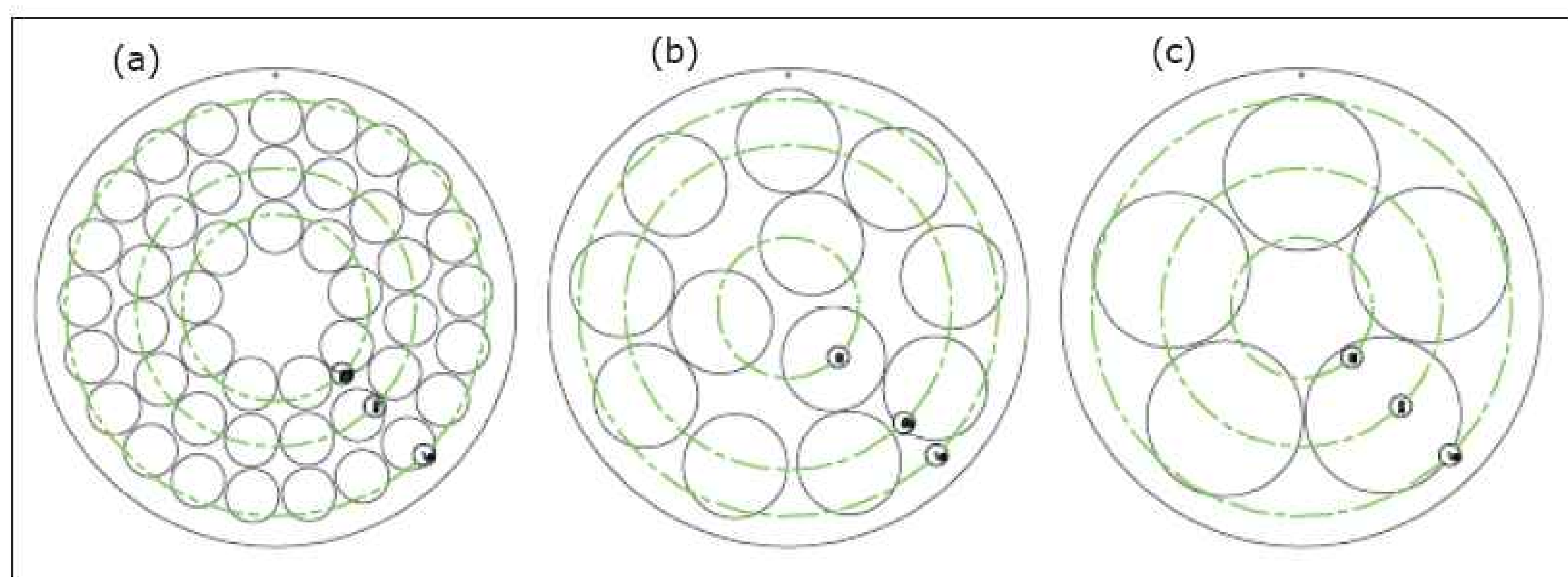

Figure 1: Typical wafer configurations on a K465 reactor for (a) 45 x 2” sapphire substrates, (b) 12 x 4” substrates, and (c) 5 x 6” substrates, along with viewport positions for in-situ sensors.

Experiment

All growths conducted in this study are on Veeco’s TurboDisc® K-465 MOCVD reactors (465mm diameter disc) utilizing ‘rimmed’ pockets machined in graphite wafer carriers coated with silicon carbide (SiC). The typical packing configuration for 2″, 4″ and 6″ wafers are illustrated in Figure 1. For this study, the 2″ sapphire substrates had a thickness of 430μm, the 4″ substrate thicknesses were 650μm and 900μm, and 6″ substrate thicknesses ranged from 900μm to 1300μm. All sapphire substrates were single-side polished with etched backsides.

In-situ curvature measurements were conducted using a Veeco DRT™-210 integrated pyrometer/reflectometer/deflectometer unit which measures along a fixed radial position within the spinning wafer carrier in the reactor, as shown in Figure 2. For curvature measurements with this device, the two-dimensional position of a reflected laser signal is measured as a wafer passes underneath the

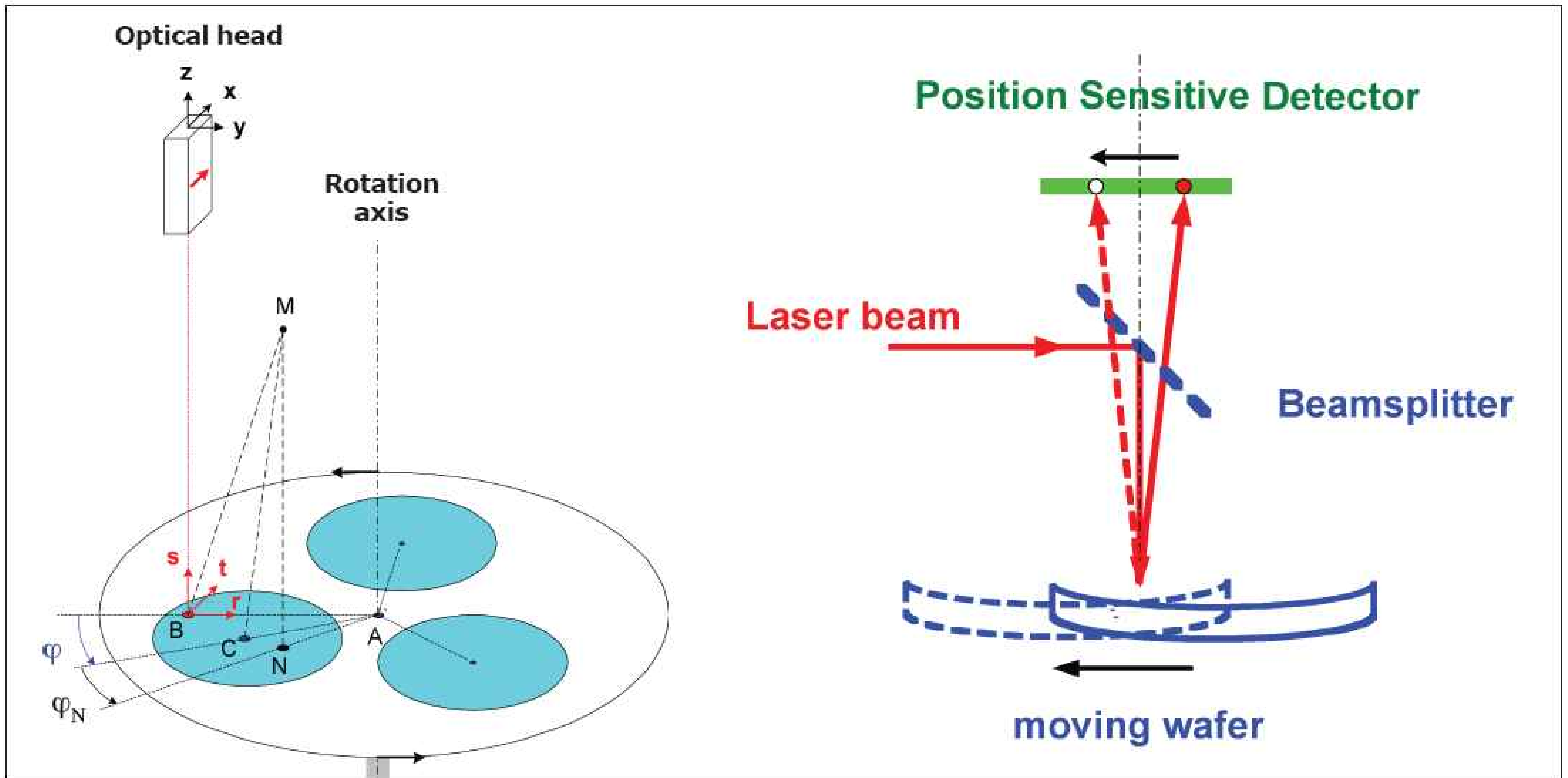

Figure 2: Schematic of single-beam deflectometer operation.

beam (normal to the wafer carrier) using a high-speed position sensitive detector. The position of the reflected beam at the plane of the detector depends on the surface local tilt angle of the wafer. As the wafer moves through the beam-path, the angle profile as a function of wafer displacement is measured, allowing the wafer curvature to be calculated. Since the single-beam deflectometer has a triangulation base determined by the wafer diameter, not the view port diameter, it has a higher resolution in curvature compared to a multi-beam deflectometer.

Curvature Evolution during LED growth

In Figure 3, we show the typical temperature, reflectance and curvature evolution of a simple 2" LED growth as a function of elapsed time. Out-of-the-box sapphire wafers are usually slightly concave. During the initial high-temperature annealing step in a hydrogen gas ambient, the wafers become more concave in shape, as their top surface expands less than that of the bottom surface, which is in thermal contact with the hot wafer carrier. Next follows either a thin (250Å), low-temperature GaN nucleation (LT-GaN, ~550ºC), where the wafers become flatter, or a high-temperature AlN nucleation layer (not shown, ~800ºC), where they remain fairly concave. After the nucleation step, thick (3–7µm) undoped and n-type GaN layers are grown, where the wafers become considerably concave, due mainly to tensile strain induced by the GaN on the wafer.

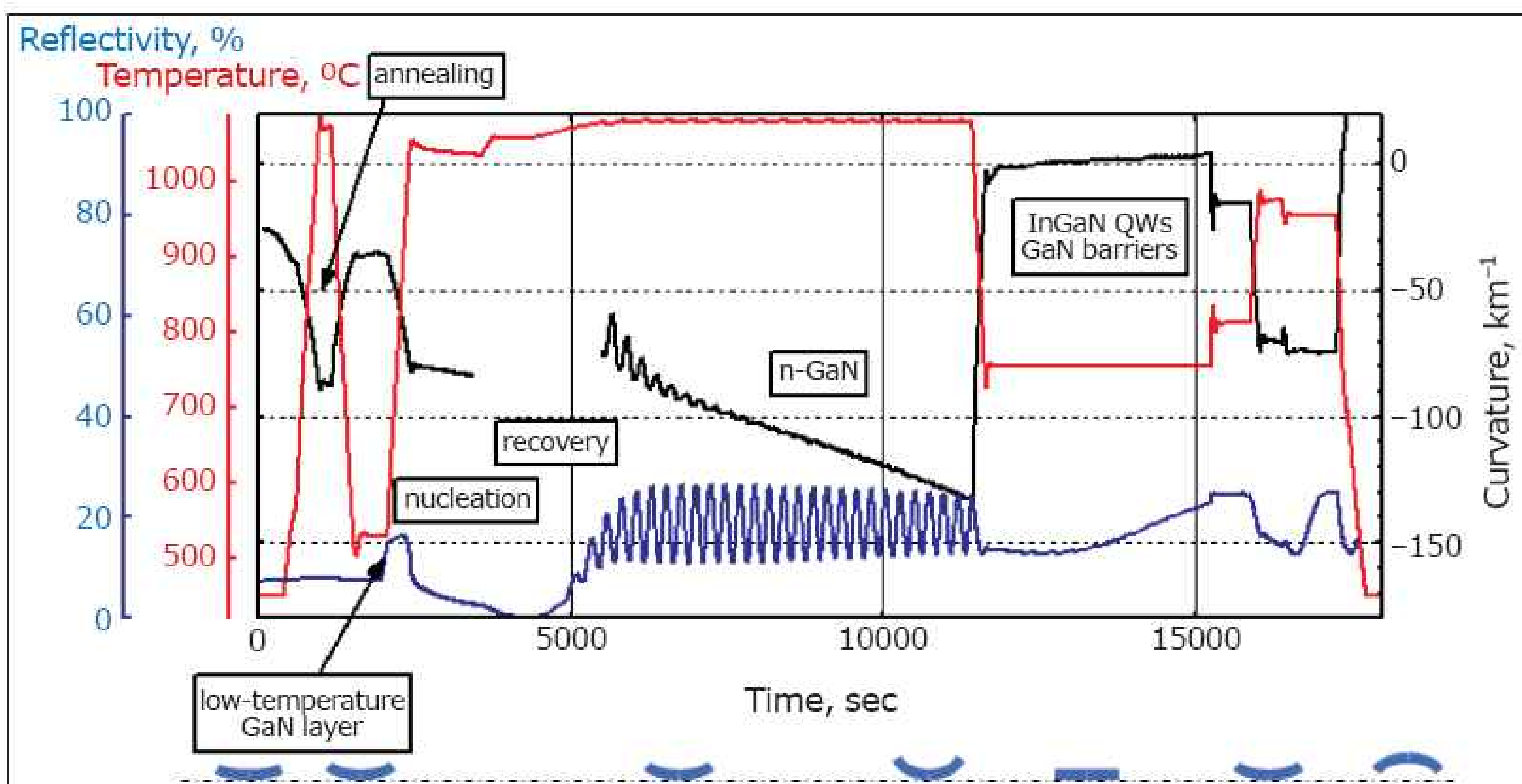

Figure 3: Growth temperature (red), reflectivity (blue) and curvature (black) as a function of elapsed time during MOCVD growth of simple LED structure.

Fortunately, during the following 25Å InGaN/130Å GaN multi-quantum-well (MQW, 5 periods) active region, the wafers flatten so that they are mildly concave or even slightly convex, due mainly to the colder deposition temperature (~750ºC) and nitrogen-only gas ambient necessary during this step. After the MQW growth, the hotter (~900ºC) p-AlGaN and p-GaN growth steps result in a concave profile, which is inverted to a convex profile when the wafers are cooled to ambient temperature.

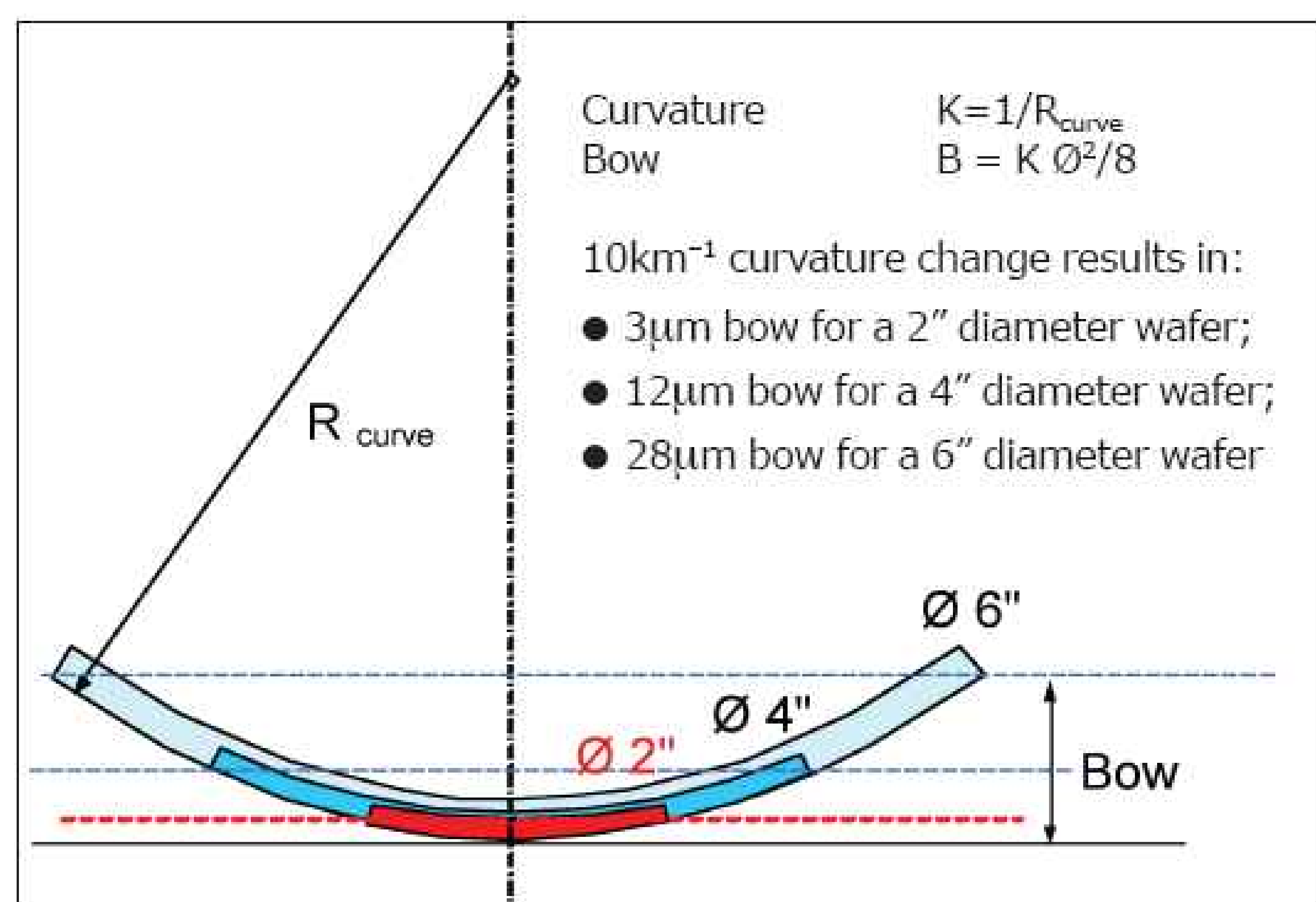

Figure 4: The relationship between the wafer curvature and bow. The bow varies as the square of the substrate diameter, Ø.

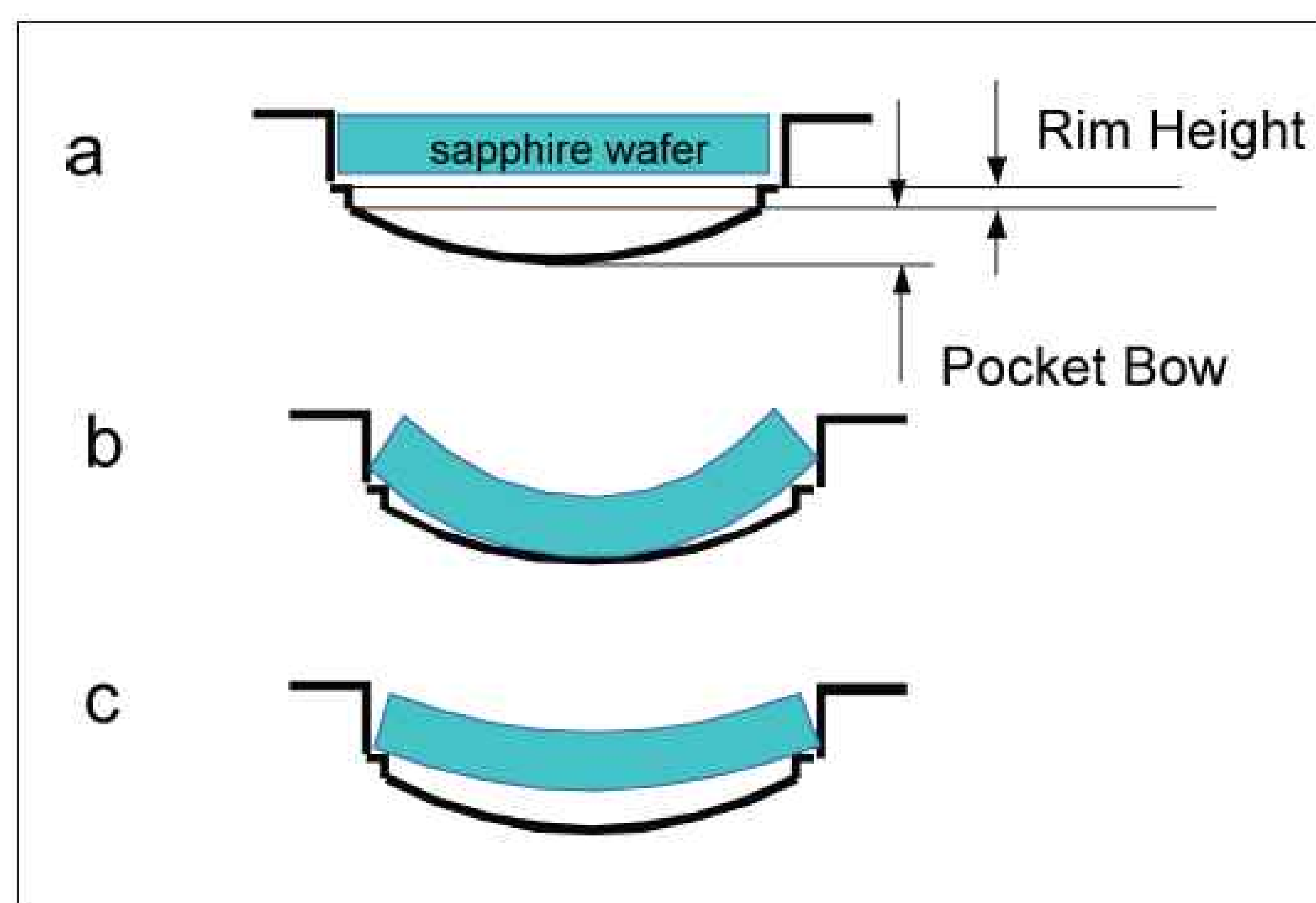

Figure 5: Rimmed pocket design geometry. Rim height and pocket bow can be independently optimized to accommodate wafer bow at end of bulk GaN layer (b), and wafer profile at InGaN MQW growth conditions (c).

Relationship between curvature and bow

The DRT-210 determines the radius of curvature of the wafer by fitting the measured profile to a parabolic curve, as shown in Figure 4.

However, a more convenient metric is the wafer bow, which is the amount of deflection of the outer radius of the wafer compared to the center.

For a given curvature, the bow varies as the square of the diameter, and thus a 4" wafer will bow four times more than a 2" wafer, and a 6" wafer will bow nine times more.

This has important consequences, which will be described in the following sections.

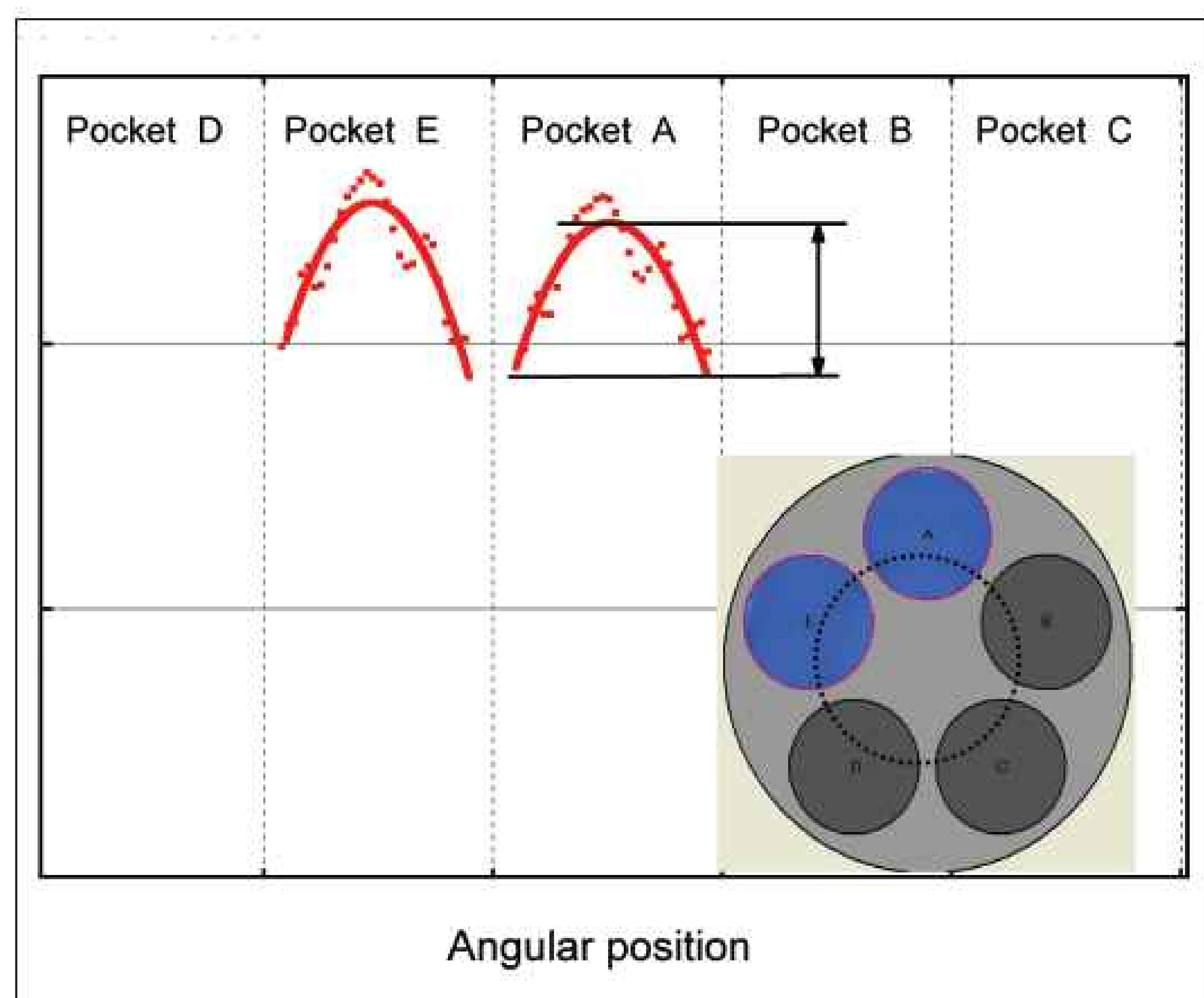

Figure 6: Temperature distribution under a sapphire wafer. The center of the pocket covered by the wafer is 6ºC hotter than the periphery for a 6" wafer, as measured by in-situ emissivity-compensated pyrometry. The difference is about 2ºC in a 4" wafer, and is not accurately measurable for a 2" diameter wafer.

Rim pocket design

Thermal uniformity within a wafer is extremely important during InGaN MQW growth, as the alloy composition is a strong function of surface temperature. The temperature dependence results from evaporation of indium from the growth surface due to the weak In-Ga bond strength. As an approximation, a 1ºC change from a nominal 750ºC growth temperature results in a 1.8nm wavelength shift for a 460nm MQW. However, this value depends upon numerous factors such as growth rate, quantum well thickness and InGaN composition, growth pressure, V/III ratio, and of course growth temperature. The heating of the wafer growth surface is primarily driven by thermal conductance within the gas ambient. Consequently, small changes in wafer bottom to pocket floor gap on the order of 10µm or more can have large effects on the thermal distribution across the wafer. Thus, it is important to tailor the pocket geometry to match the wafer shape during the active layer.

As is evident in Figure 3, the wafer curvature changes significantly during the GaN and InGaN growth layers. To compensate for these differences, we have developed a rim pocket design that allows independent optimization of the rim height and floor geometry, as illustrated in Figure 5. The pocket rim height is chosen to accommodate the large concave bow that occurs during GaN growth, whereas the pocket floor shape (concave, convex, or flat) is profiled to give uniform temperature distribution within-wafer during the critical InGaN MQW growth.

Another effect that must be taken into account when optimizing within-wafer thermal uniformity is the difference in temperature between the center and the outer radius of the wafers, as shown in Figure 6. The thermal delta is due to a blanketing effect of the wafer located on the top surface of the hot pocket surface.

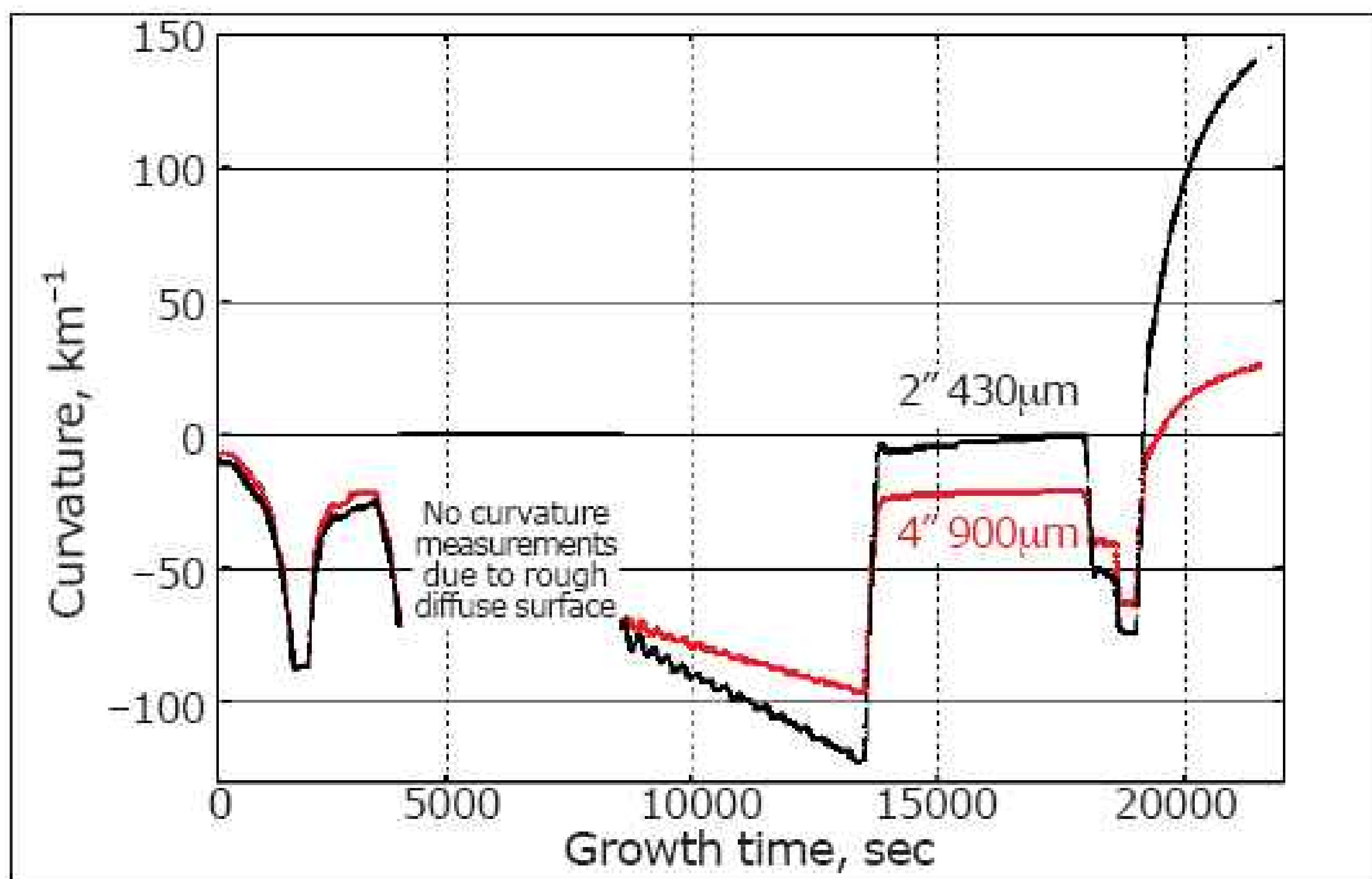

Figure 7: Wafer curvature as a function of elapsed time during MOCVD growth of equivalent simple LED structures on 2″ 430µm-thick and 4″ 900µm-thick sapphire substrates.

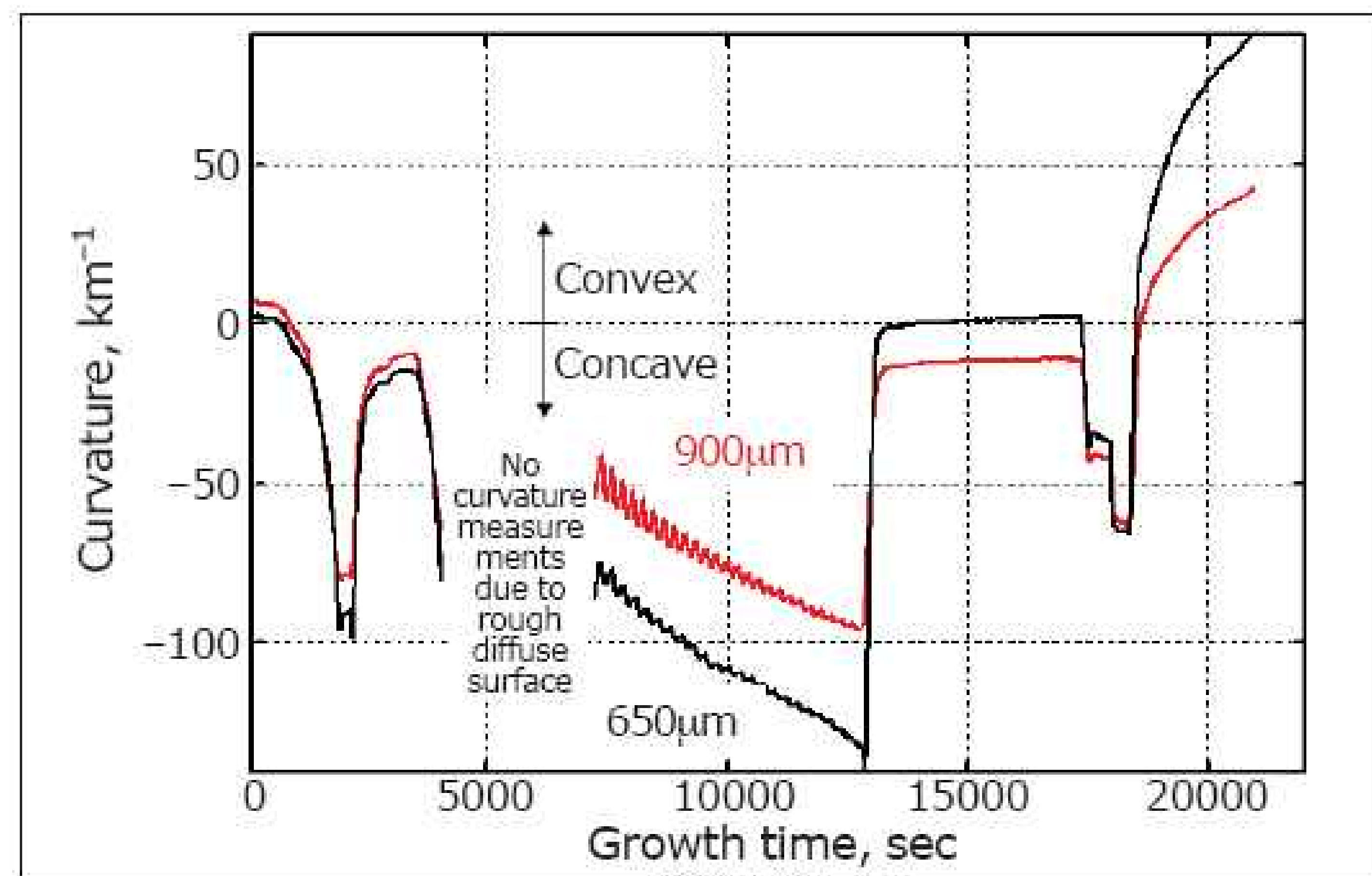

Figure 8: Comparison of curvature for 4″ LED structures with 650µm- (black) and 900µm- (red) thick substrates utilizing an equivalent growth recipe.

This phenomenon becomes more dominant as the area-to-circumference ratio becomes larger, as is the case with larger wafer sizes.

2″ and 4″ LED growth

In Figure 7, LED growths on 430µm-thick 2″ and 900µm-thick 4″ wafers are compared. The resulting slope in the bulk n-GaN layers towards increasing curvature is related to the thickness of the substrates. At the end of the 3.5µm n-GaN layers, the 2″ wafer curvature is $-110km^{-1}$, corresponding to a concavity of 34µm, whereas the 4″ wafer curvature is less at $-95km^{-1}$, but corresponding to a larger concavity of 118µm. Even though the curvature is greater for the 2″ wafers in the GaN layers, at the InGaN growth conditions the wafer becomes nominally flat (curvature $\sim 0km^{-1}$), such that a flat pocket floor profile will give a uniform temperature distribution across the wafer. Conversely, the 4″ wafer remains concave at $-25km^{-1}$, corresponding to a concavity of 31µm at the active layer. Thus, for this 4″ growth, a relatively concave pocket floor is needed to thermally compensate the 4″ curvature combined with the 2°C difference induced by the thermal blanketing effect.

The curvature evolution for 4″ MQWs and LEDs with 650µm and 900µm sapphire substrates using the same recipe are shown in Figure 8. As expected, during the high-temperature GaN layers, the difference in curvature profiles start to diverge drastically. At the end of 4µm of n-GaN, the 650µm sapphire substrate has a curvature of $-133km^{-1}$ (black), whereas the 900 mm sapphire substrate ends at $-95km^{-1}$ (red), corresponding to bow values of 165µm and 118µm, respectively.

This difference in film strain from the thick GaN makes a large difference in thermal uniformity when the wafers are cooled to the active layer growth conditions. The 650µm sapphire substrate is nominally flat at the start of the MQW growth, whereas the 900µm sapphire substrate has a $-13km^{-1}$ curvature, corresponding to a 16µm concave bow. In order to achieve optimal within-wafer wavelength uniformity for these different substrate thicknesses with this particular recipe, rim pockets with a 175µm rim depth and a flat floor profile are necessary for the 650µm substrates, however a floor profile of ~25µm concavity is optimal for the 900µm-thick substrates.

6″ LED growth

We initially started with the equivalent LED growth process on 6″ wafers that worked well for the 2″ and 4″ diameter substrates. However, we found that thin 6″ substrates (<1000µm) caused problems, primarily due to extensive wafer bow occurring during the initial low-temperature GaN nucleation and subsequent GaN buffer steps. We observed that, if the wafers incur a concave bow of greater than about 300µm, a huge thermal gradient is created between the center and the outer radius of the pockets, which often results in wafer cracking. In order to resolve this issue, we reduced the amount of film stress within the wafer by nucleating with high-temperature AlN instead of the low-temperature GaN. In addition, to minimize thermal gradients across the wafer created by non-equilibrium heating or cooling, slower temperature ramps were utilized for the 6″ growths during the highly concave GaN layers. As a result, 900µm- and 1mm-thick substrates can be used with this kind of approach without cracking. However, the within-wafer uniformity results tended to be irreproducible, possibly due to subtle differences in the thickness control of the substrates or differences in sapphire internal stress or flexural strength. Regardless of the growth technique or film structure, obtaining repeatable MQW wavelength uniformity proved considerably more challenging for these thin wafers due to the extreme curvature generated between the GaN and MQW growth conditions.

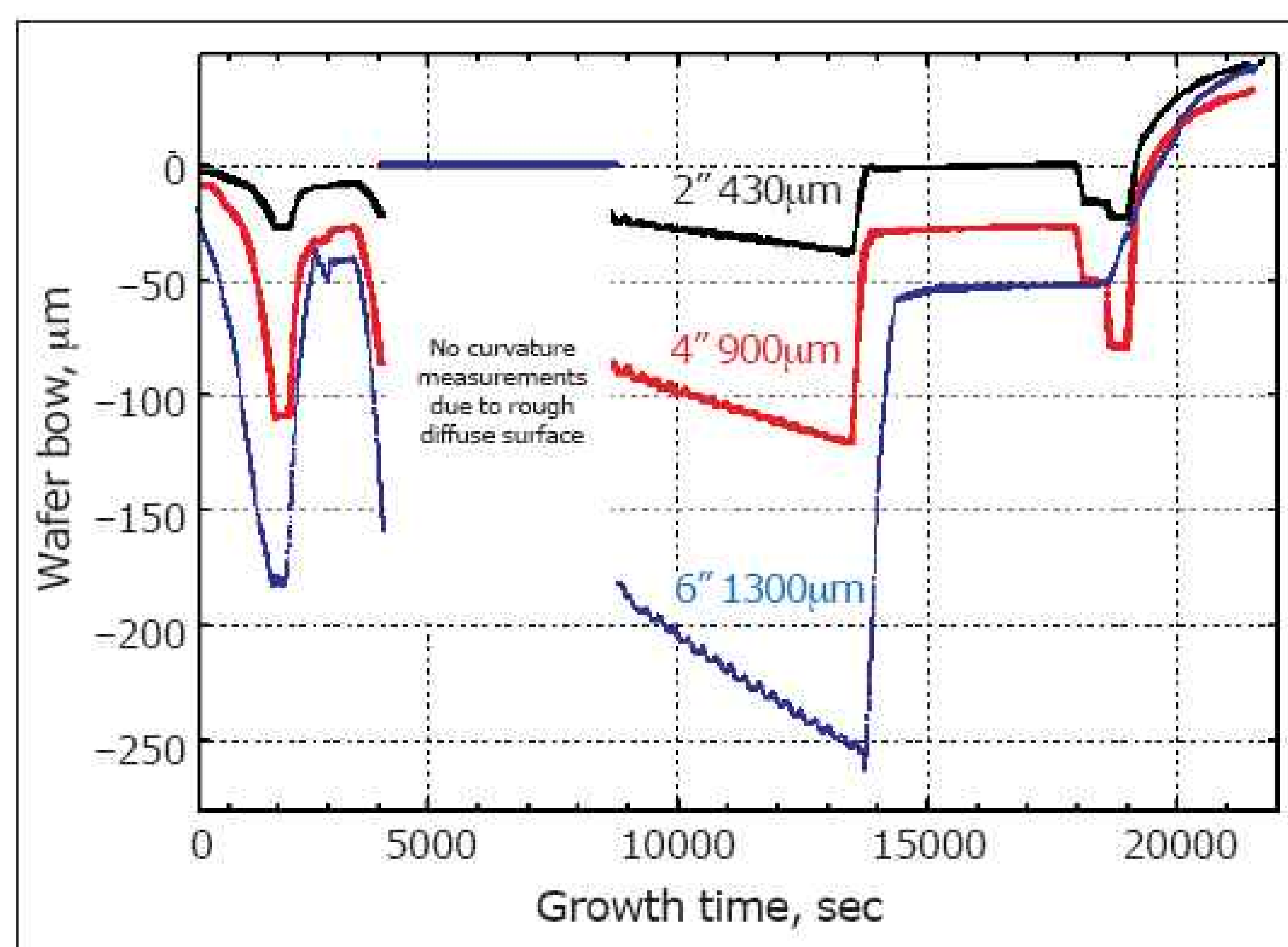

Figure 9: Comparison of wafer bow for 2″, 4″ and 6″ wafers in equivalent growth recipes. All bows in this example are concave in shape.

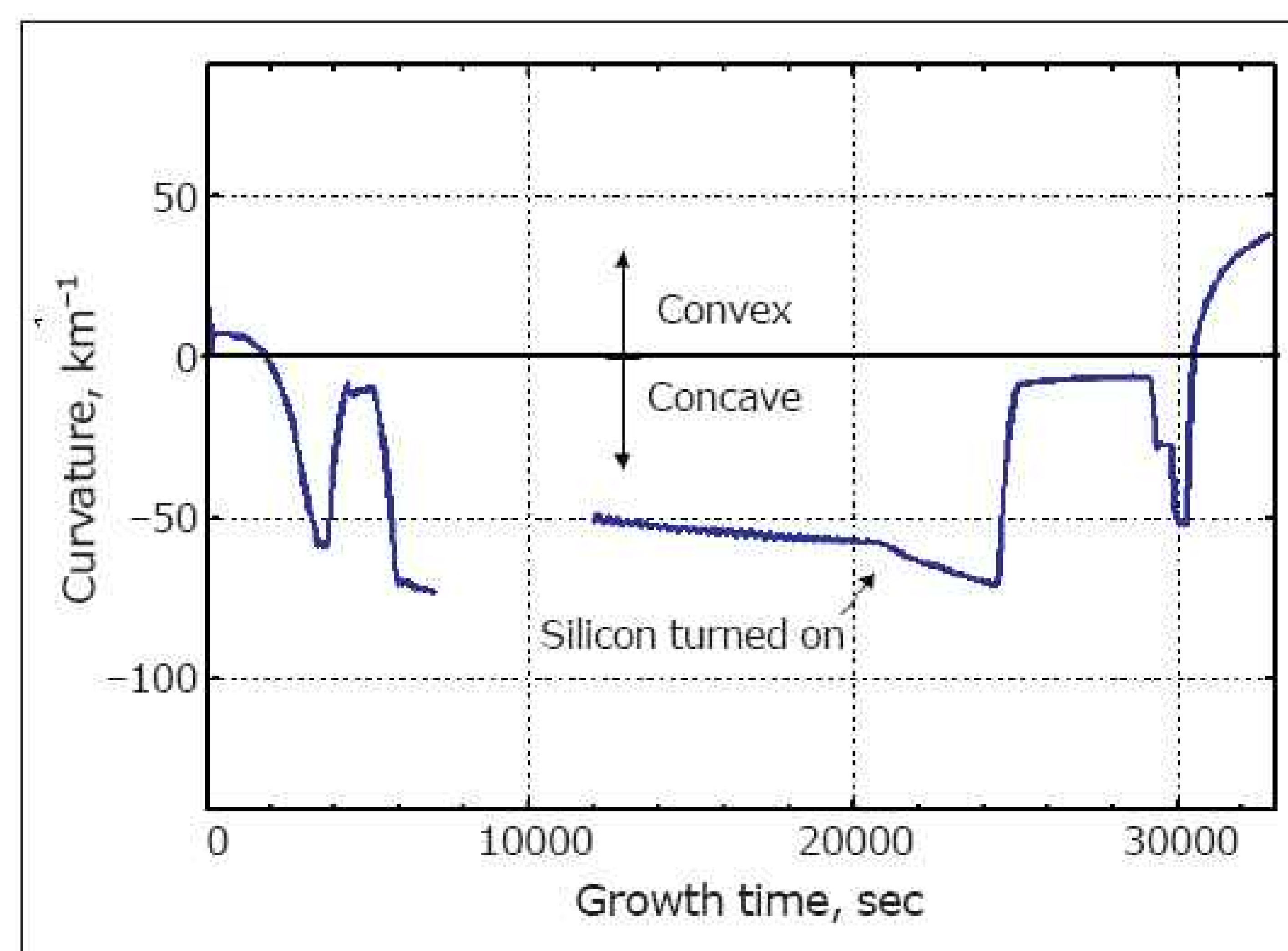

Figure 10: Curvature evolution of a simple blue LED on 1.3mm thick 6″ sapphire using AlGaN nucleation, and thick undoped GaN layer before n-GaN layer growth.

Unlike their thinner counterparts, 1.1mm- and 1.3mm-thick 6″ diameter substrates exhibited much more rigidity and gave much more reproducible run-to-run curvature profiles. At a thickness of 1.3mm, growth processes similar to the 4″ diameter wafers could be implemented without the need to precisely bin individual wafer thicknesses. In Figure 9, we compare the wafer bow evolution for the 2″, 4″ and thicker 6″ wafers in the study. Note that, even with the 1.3mm-thick 6″ wafers, the bow is still about 270µm at the end of a 3.5µm-thick n-GaN layer when a LT-GaN nucleation method is used.

Figure 10 shows the reflectance and wafer curvature profile for a 6″ LED growth on a 1.3mm-thick substrate, with AlGaN nucleation and a thick undoped GaN buffer, which gives less curvature than GaN nucleation and a thick n-GaN buffer. As the silicon dopant is introduced to the GaN layers at a time of 21,000s, the curvature slope becomes more negative. At the end of the 6µm-thick bulk GaN layer, the curvature is $-70km^{-1}$, which is much less than for 2″ and 4″. However, even though the curvature is less, the actual concavity is still about 195µm.

Using our in-situ curvature measurements, we have developed wafer carrier pocket profiles that allow for the large bows during the GaN growth while optimizing bottom pocket shapes that conform to the curvature of the 6″ wafers during the InGaN MQW growth. By understanding these dynamics, good within-wafer wavelength uniformity of $\sigma < 2nm$ can be achieved on 6″ wafers, as shown in Figure 11, which is similar to what can be achieved on 2″ and 4″ diameter wafers.

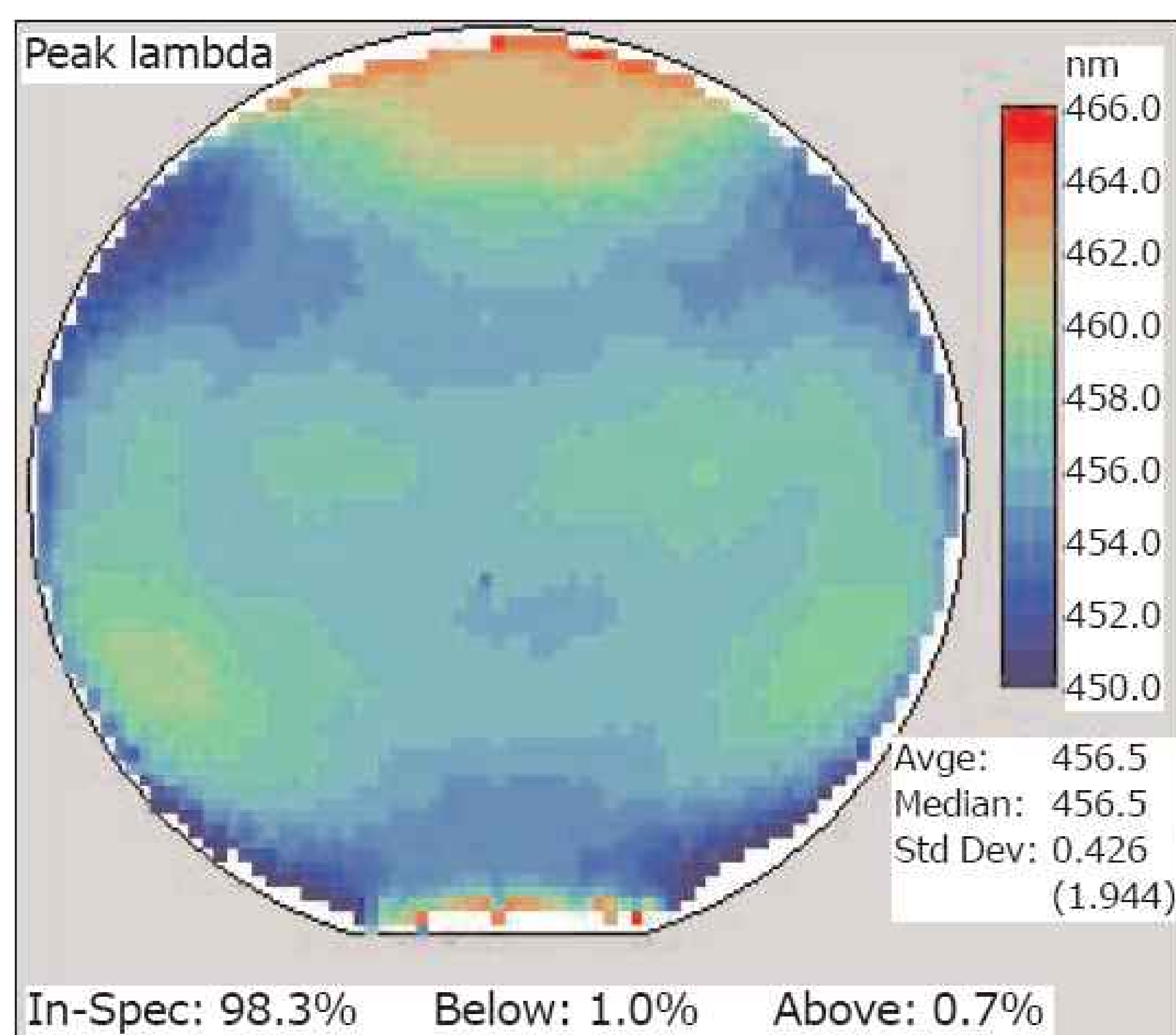

Figure 11: PL map of 1.3mm-thick, 6″ sapphire substrate showing within-wafer wavelength uniformity (1mm edge exclusion) for five-period MQW with 6µm GaN buffer.

Summary

Understanding the dynamics of wafer curvature is required for process development of LED epitaxy, especially for larger wafer sizes. Subtle changes in nucleation, bulk GaN thickness and doping as well as growth temperature can have strong effects on the curvature of the wafers during the growth process. A standard growth process can be used for wafer sizes from 2″ to 6″, provided that the 6″ wafers are at least 1.1mm thick. The use of thinner 6″ wafers will need additional research and development, both at the MOCVD epitaxy and substrate quality level.

The concepts learned in the 6″ development process can be adapted to even larger wafer sizes, such as 8″. Our Veeco K-465 reactor has a common chamber configuration for all different size wafers, from 2″ to 8″, so continued increases in wafer size for research and production can be realized quite easily in the future. ■

Authors: E. Armour, F. Lu, M. Belousov, D. Lee, and W. Quinn
Veeco Instruments Inc, Somerset, NJ, USA